A Multi-Service System-On-Chip Including On-Chip Memory With Multiple Access Paths

5 ## ABSTRACT OF THE DISCLOSURE

In an integrated circuit, a memory unit includes a first and a second data transfer interface. The first data interface services successive first accesses by a processor and subsystem of the IC, whereas the second data interface services

10 second accesses by at least the processor in parallel. In one embodiment, the accesses are properly sequenced and responded to.